

The Core Clock System for the Next Generation Itanium™ Microprocessor

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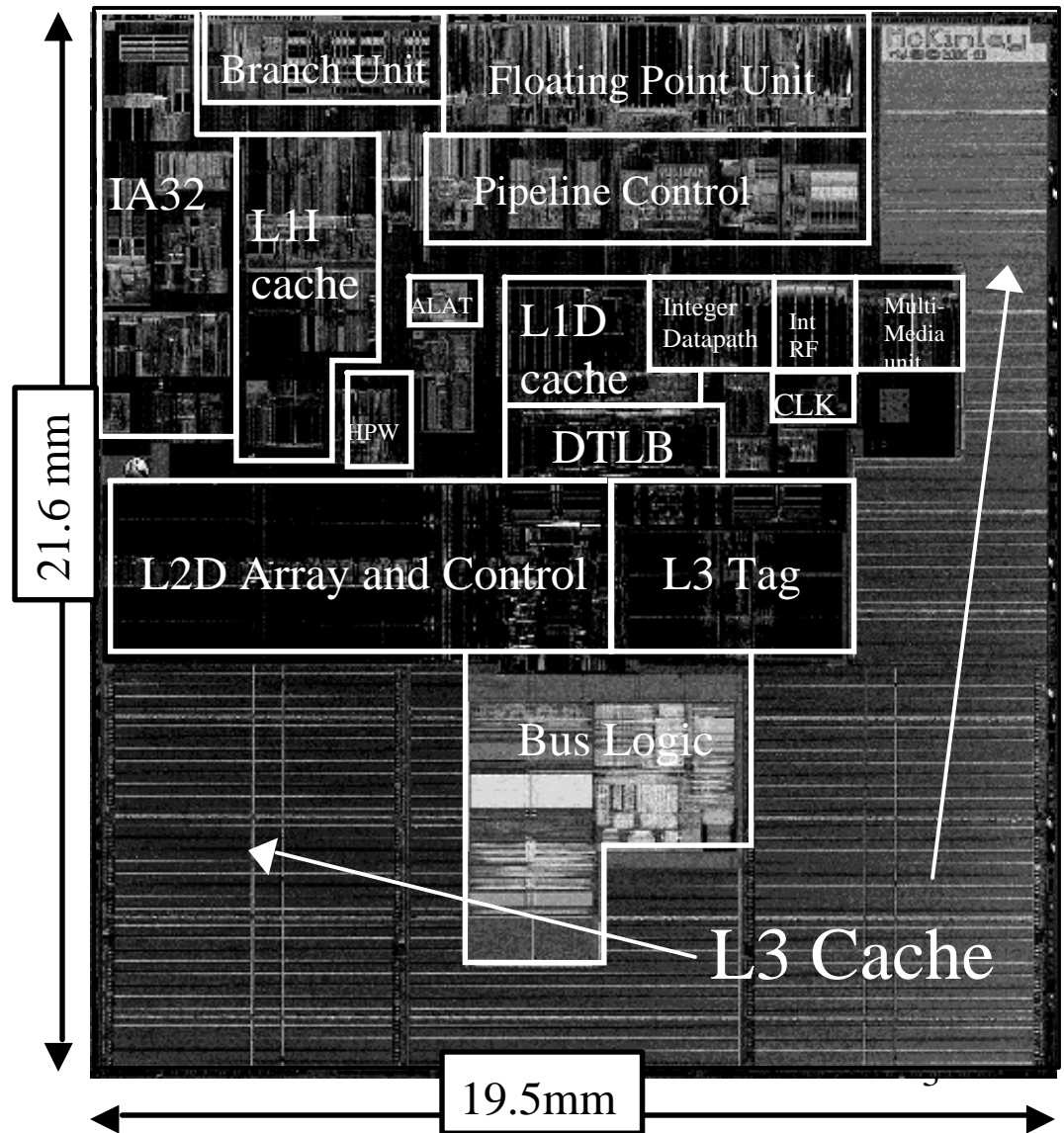
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Topics

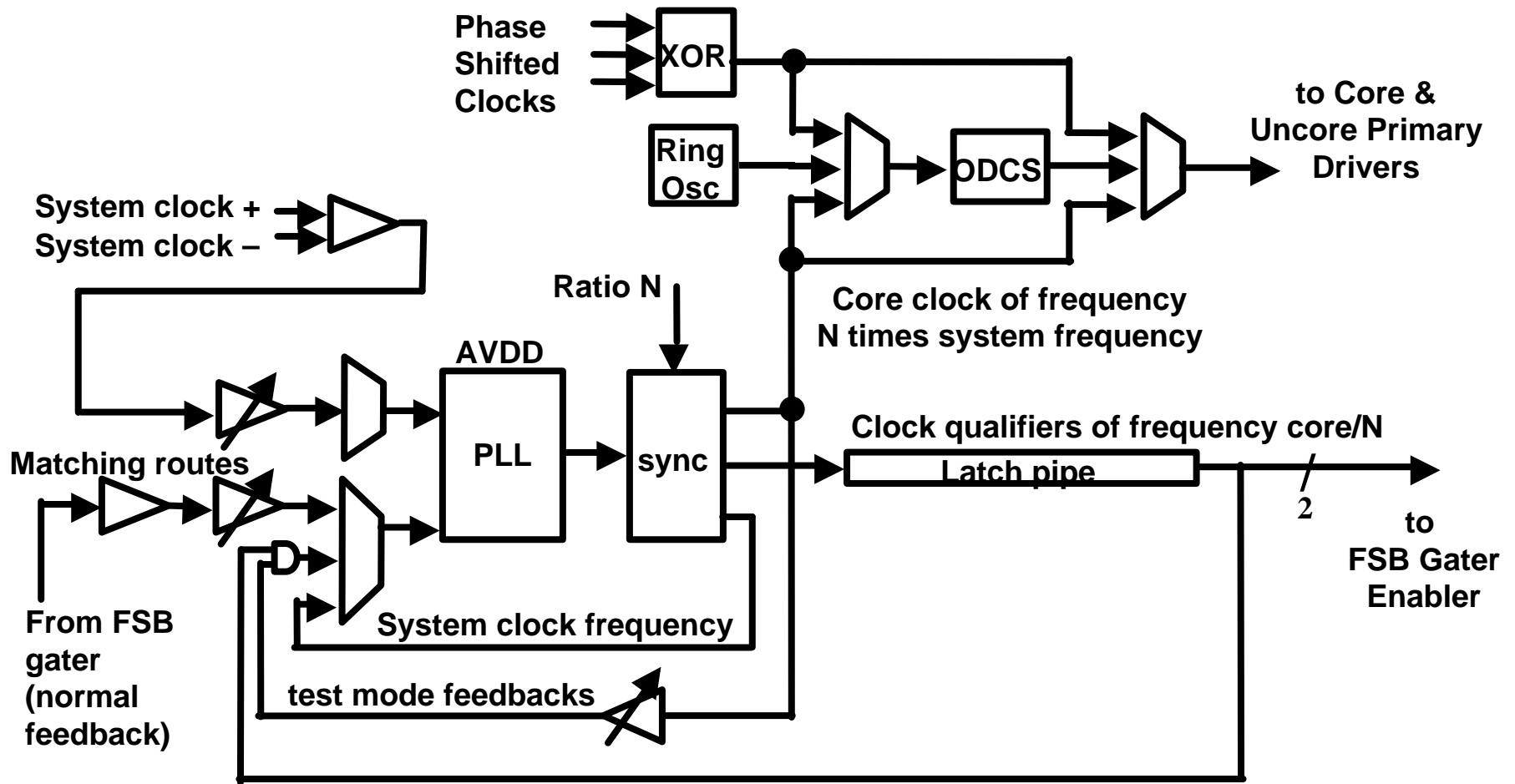
- McKinley floorplan
- Clock generation
- Clock distribution
- Clock repeaters
- Routing tool
- Summary

McKinley Floorplan

- 0.18 μm , AI process
- 200MHz system clock
- 1GHz core clock
- Core clocking:
 - 260 mm²
 - 1 primary driver
 - 5 repeaters
 - 33 delay SLCBs
 - 18k gated buffers
 - 157k clocked latches



Clock Generation

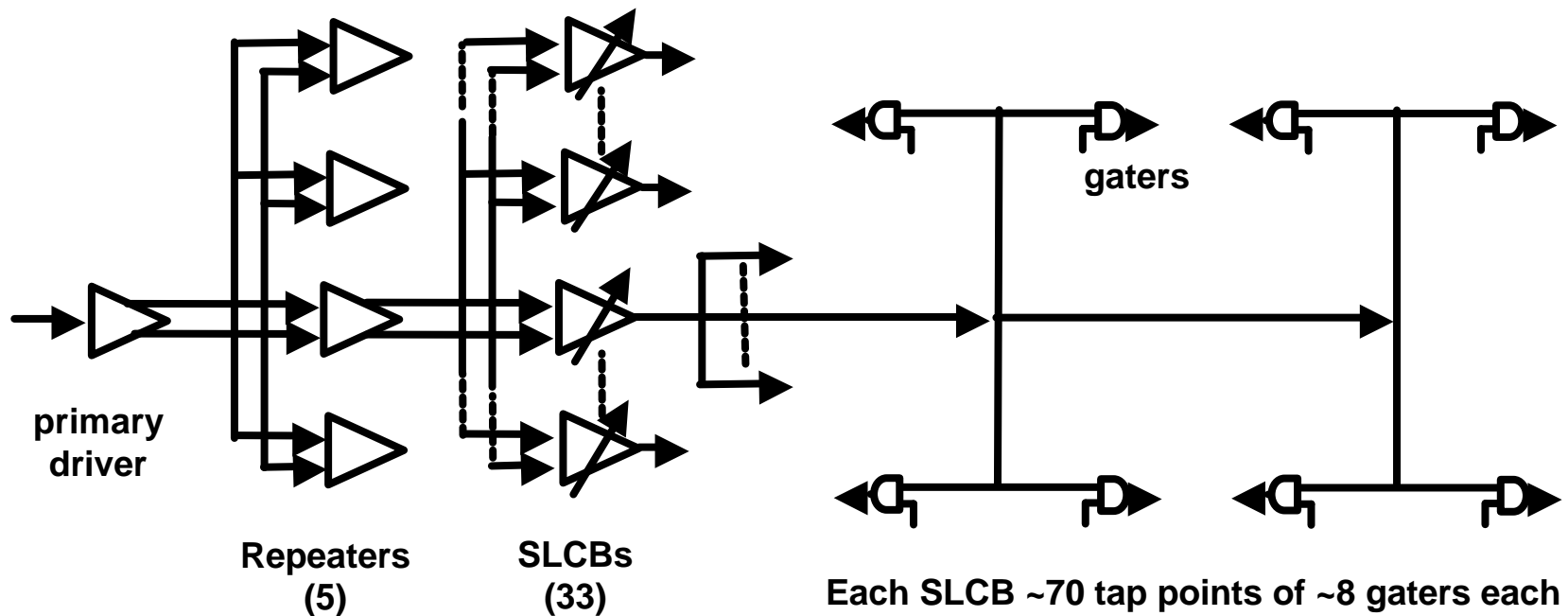


Clock Generation

- System clock characterization
 - 60-250MHz
- PLL characterization
 - Up to 1.6GHz at 1.5V
 - Up to 2.0GHz at 2.0V
- Core clock characterization
 - Up to 1.4GHz at 1.5V
 - Up to 1.7GHz at 2.0V
- PLL unaffected by ODCS and stop clock
- Ring oscillator allows known initial conditions

Core Clock Distribution

- **First level:** Pseudo-differential, impedance matched branching, balanced h-tree
- **Second level:** balanced, width and length tuned binary h-tree
- **SLCB:** adjustable delay buffer
- **Gaters:** all constant input loading with load-tuned drive strength



SLCB Schematic

The schematic illustrates the SLCB (Signal Level Control Block) architecture, which is divided into two main sections: coarse control and fine control.

Coarse Control: This section takes an input signal (labeled $/2$) and processes it through a series of three inverters. The output of the third inverter is fed into a multiplexer. The multiplexer also receives feedback signals from the first two inverters. The output of the multiplexer is then fed into a differential pair of transistors, which produces the coarse control output (labeled $/2$).

Fine Control: This section is shown in a dashed box and provides a detailed view of the differential pair's load network. The top network consists of three PMOS transistors with gain factors of 4x, 2x, and 1x, connected in parallel. The bottom network consists of three NMOS transistors with gain factors of 4x, 2x, and 1x, connected in parallel. The differential pair's output is labeled $/2$.

Delay and Clock Distribution: A delay block (labeled $/5$) is connected to the input of the coarse control stage. A clock distribution block (labeled $/2$) is connected to the input of the fine control stage. The output of the fine control stage is labeled $/2$.

Debug Mode: A debug mode input is connected to the multiplexer in the coarse control stage, allowing for signal monitoring.

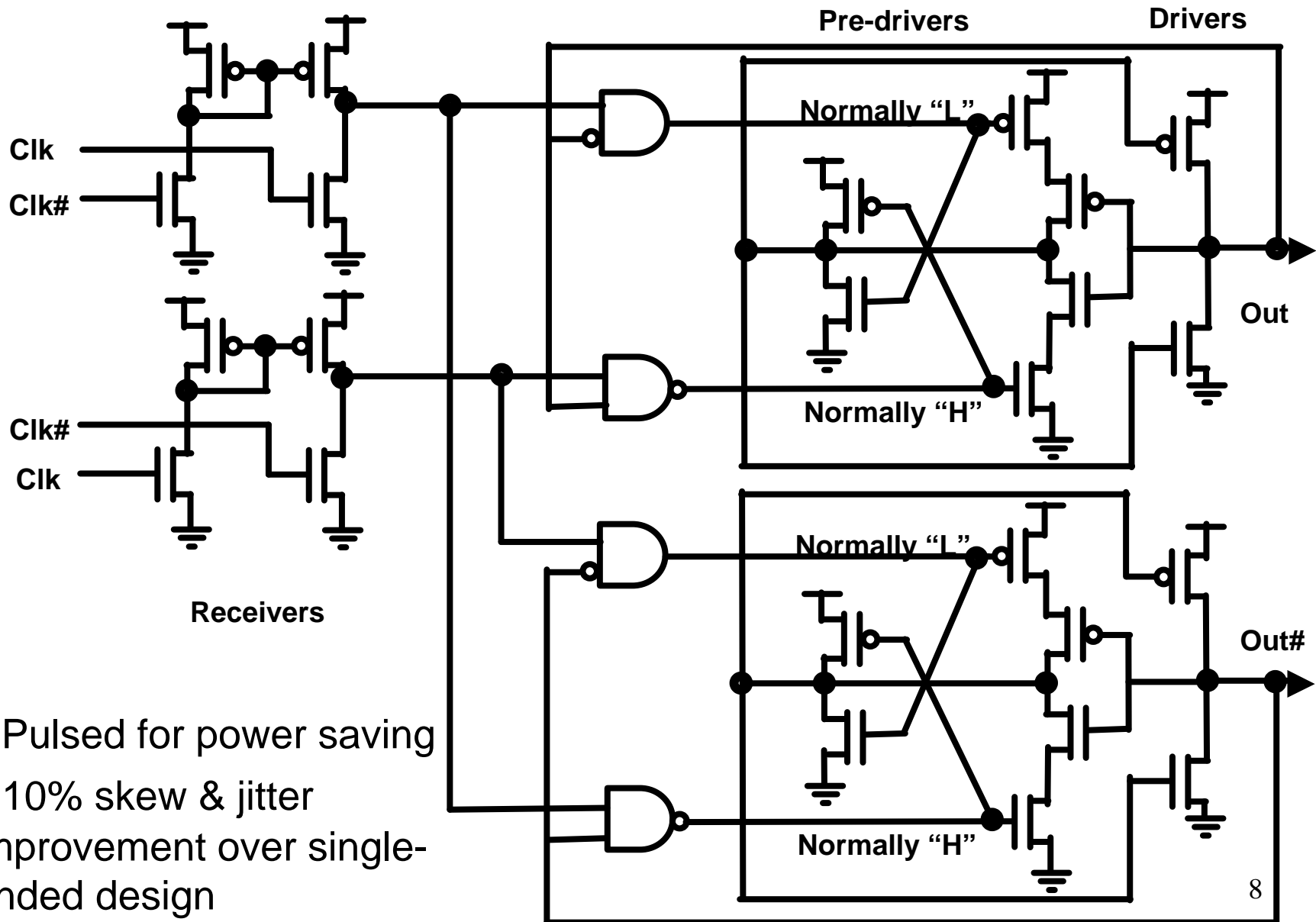
Output: The final output of the SLCB is labeled "To gates" and is connected to a multiplexer (labeled 1 and 0) which selects between the coarse control output and the debug mode input. The output of this multiplexer is then fed into a final inverter (labeled $/2$) to produce the final signal.

- 256ps delay range for debug purposes

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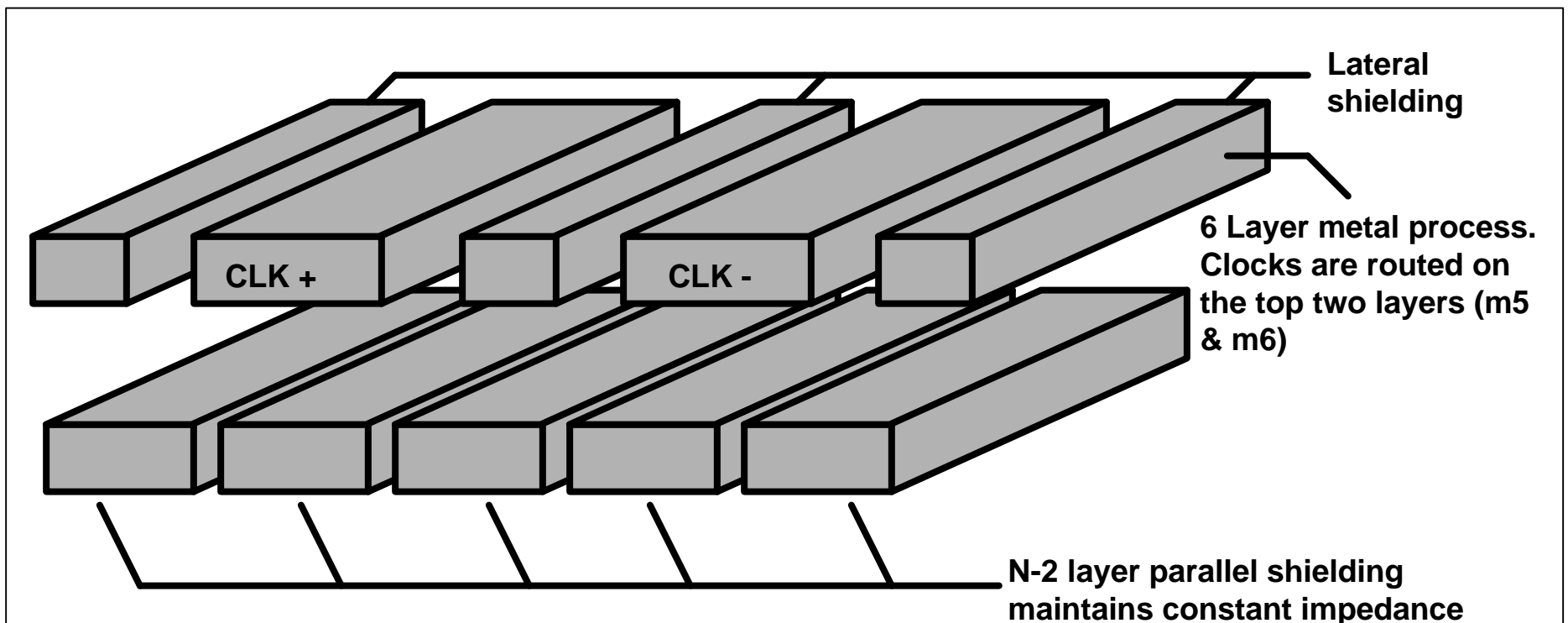
Clock Repeater



- Pulsed for power saving
- 10% skew & jitter improvement over single-ended design

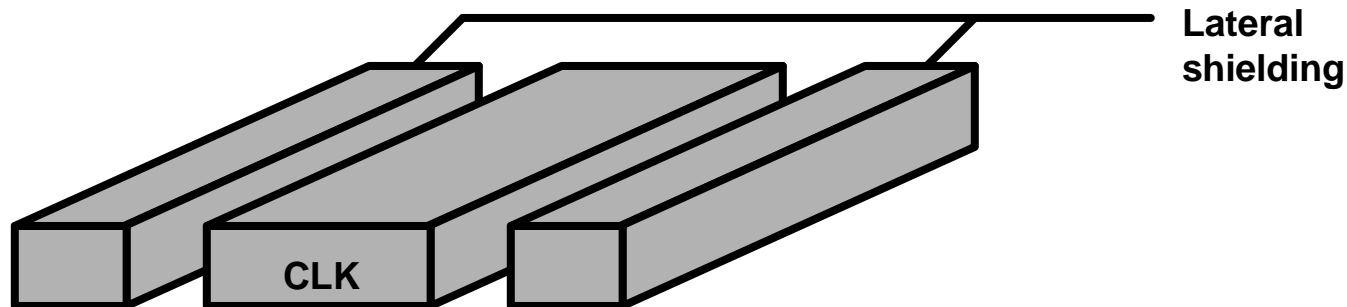
First Level Route Geometry

- Balanced h-tree with impedance matched branching
- 0.8 to 12 μm tuned widths for impedance matching
- N-2 shielding controls transmission-line effects, noise injection, and simplifies modeling

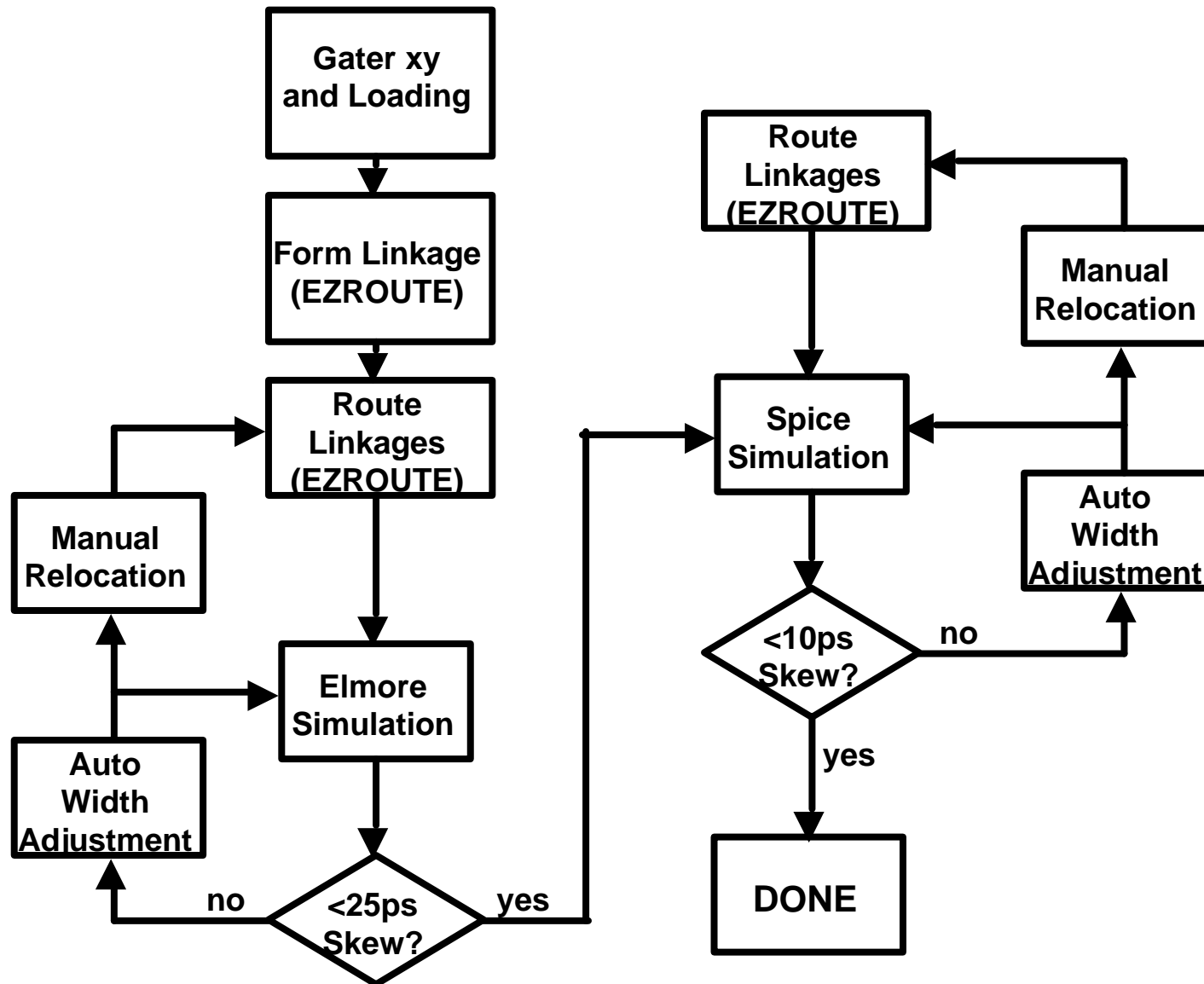


Second Level Route Geometry

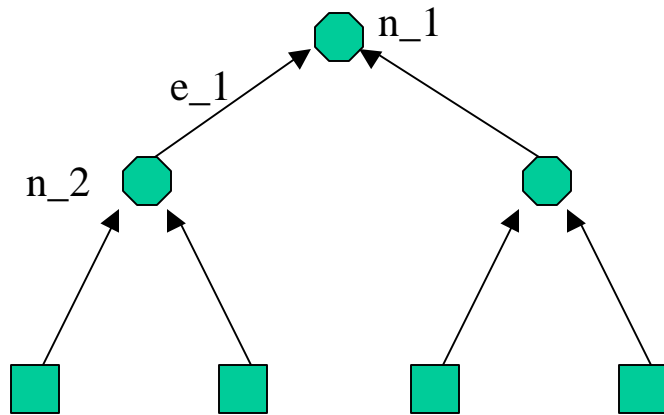
- Balanced, width and length tuned binary h-tree for minimal skew and power dissipation
- Wire widths from .88 to $6\mu\text{m}$
- Multiple variations of gaters, all with input loads of 7.75fF
- Gater output drive strengths tuned to load
- ~70 tap points per SLCB
- ~8 gaters per tap
- ~4.5pF gater loading per SLCB
- ~18pF gater + wire load per SLCB



Level 2 Routing Flow Diagram



Data Representation of Level 2 Route



■ **Tap Node:** Location and routes to local gates determined by block designer.

● **Branch Node:** Location of branch in route determined by tool.

→ **Link:** Width and length of route determine by tool.

De-skew Algorithm applied per iteration:

$AvgD(n)$ = Average of children delays

$ActD(n)$ = Actual (simulated) delay from the node up to the SLCB

$Wid(e)$ = metal width of the route

$Del(e)$ = delay between nodes connected by the link

$Del2Wid(e, delay)$ = estimated width for desired Elmore delay

$CONST$ = convergence factor

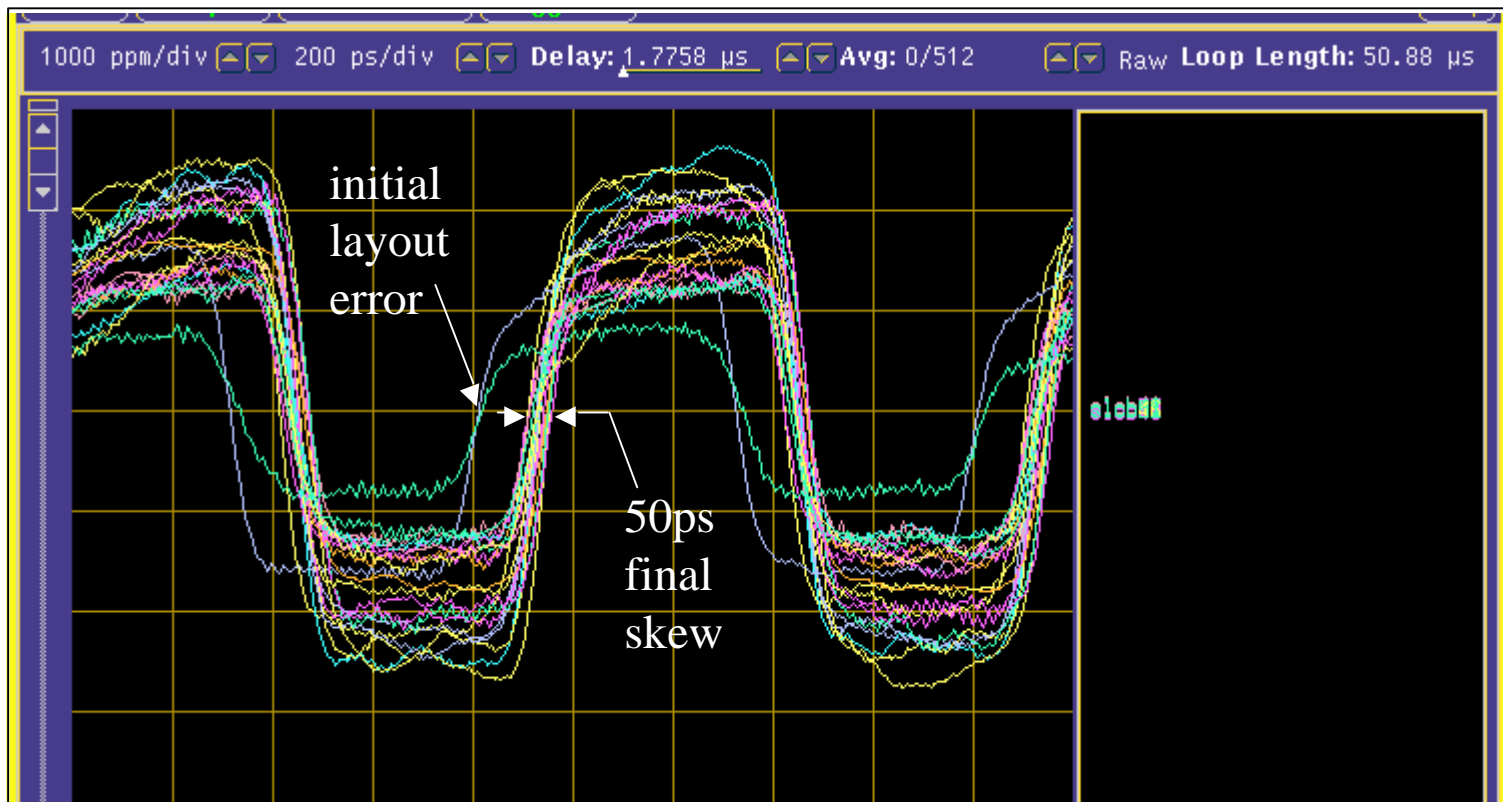
$$Wid(e_1) = Del2Wid(Del(e_1) + CONST * ActD(n_2) * (1 - AvgD(n_1)/AvgD(n_2)))$$

Second Level Clock Routing Tool

- EZroute tool created for balanced h-tree creation
- Elmore models create first order RC delay
- Spice models for accurate results
- Tool iterates bottoms-up across core to obtain lowest skew
- Manual intervention applied where tool cannot resolve
- Minimal engineer restriction to gater placement
- Minimal Loading relative to grid design
- Elimination of grid allows deskew for debug of critical paths

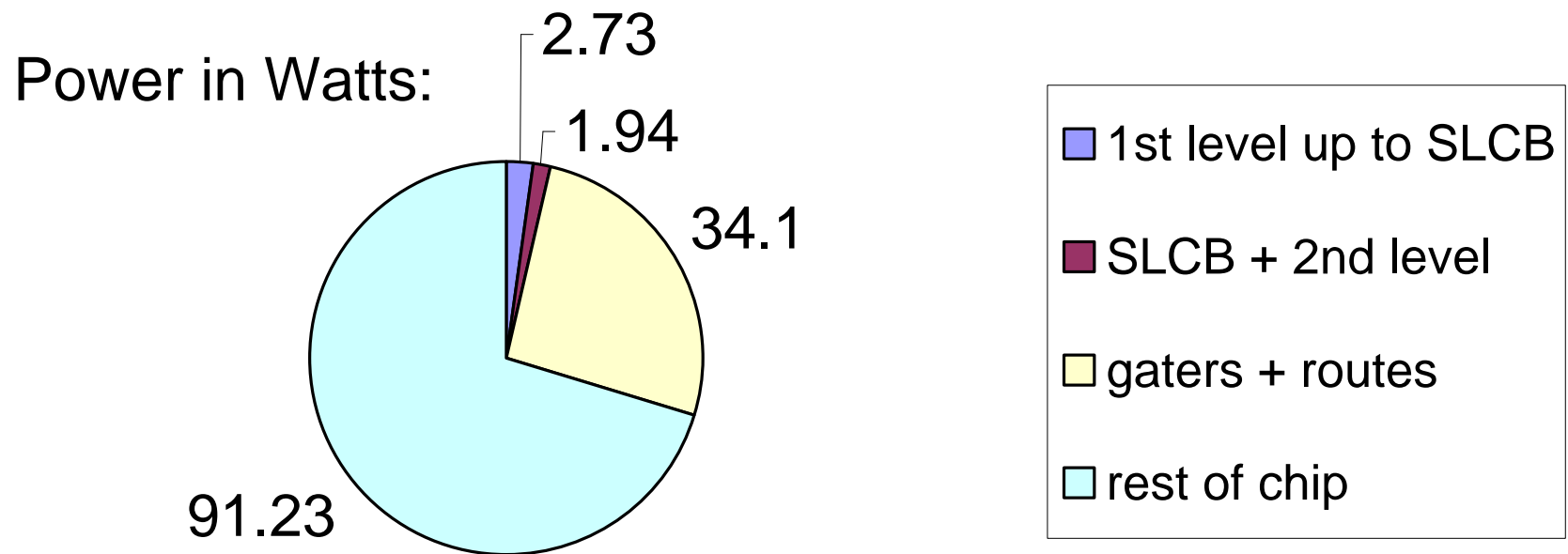
Measured Skew

- Laser probed SLCB skew (non-loading, but invalid DC levels)
- 2 SLCBs outside of expected range due to layout error
- Initially fixed via scan, then with mask change



Total Chip Power Dissipation

- 30% of 130W chip power is clock distribution
- Estimate up to 47% clock distribution power if using grid depending on hierarchy and sparseness of grid



Summary

- A balanced h-tree clock distribution without grid has been realized on a large processor.
- Intentional skewing allows for debug
- Proprietary clock distribution software created (EZroute) to ease the traditionally time consuming task of balanced h-tree layout.
- Elmore models used for quick initial results
- 30% of chip power is dissipated in distribution
- 62ps across-core skew obtained at 1GHz